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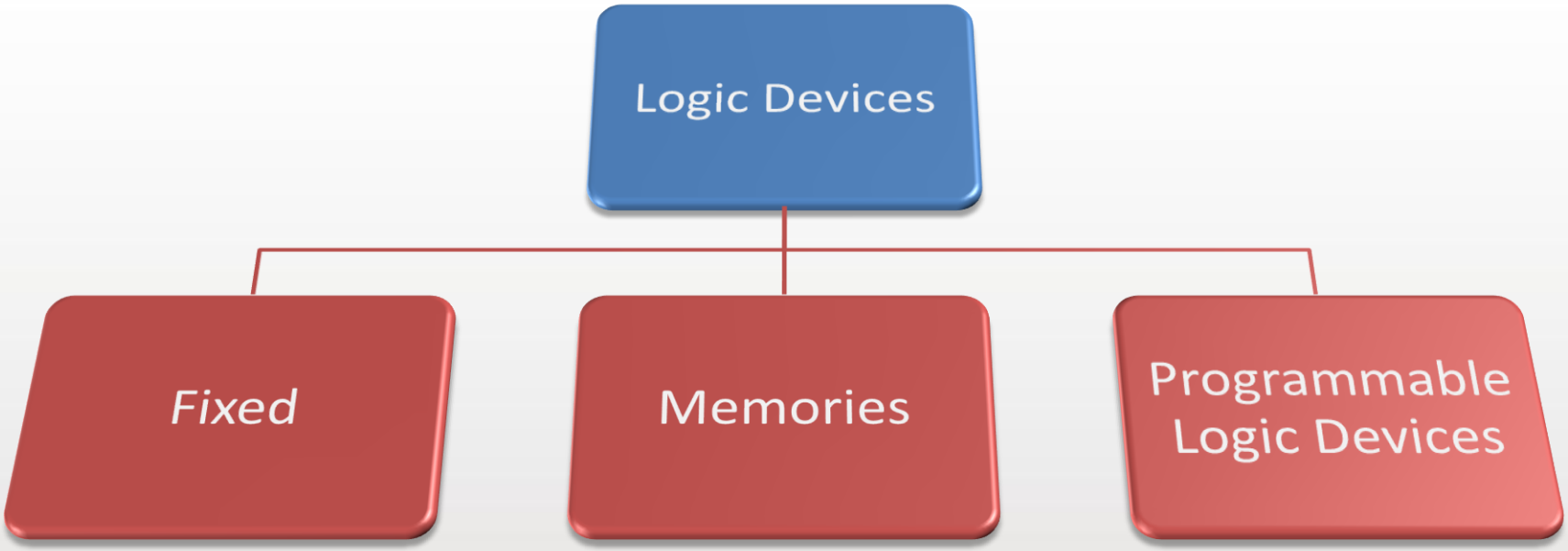
ONLINE LEARNING

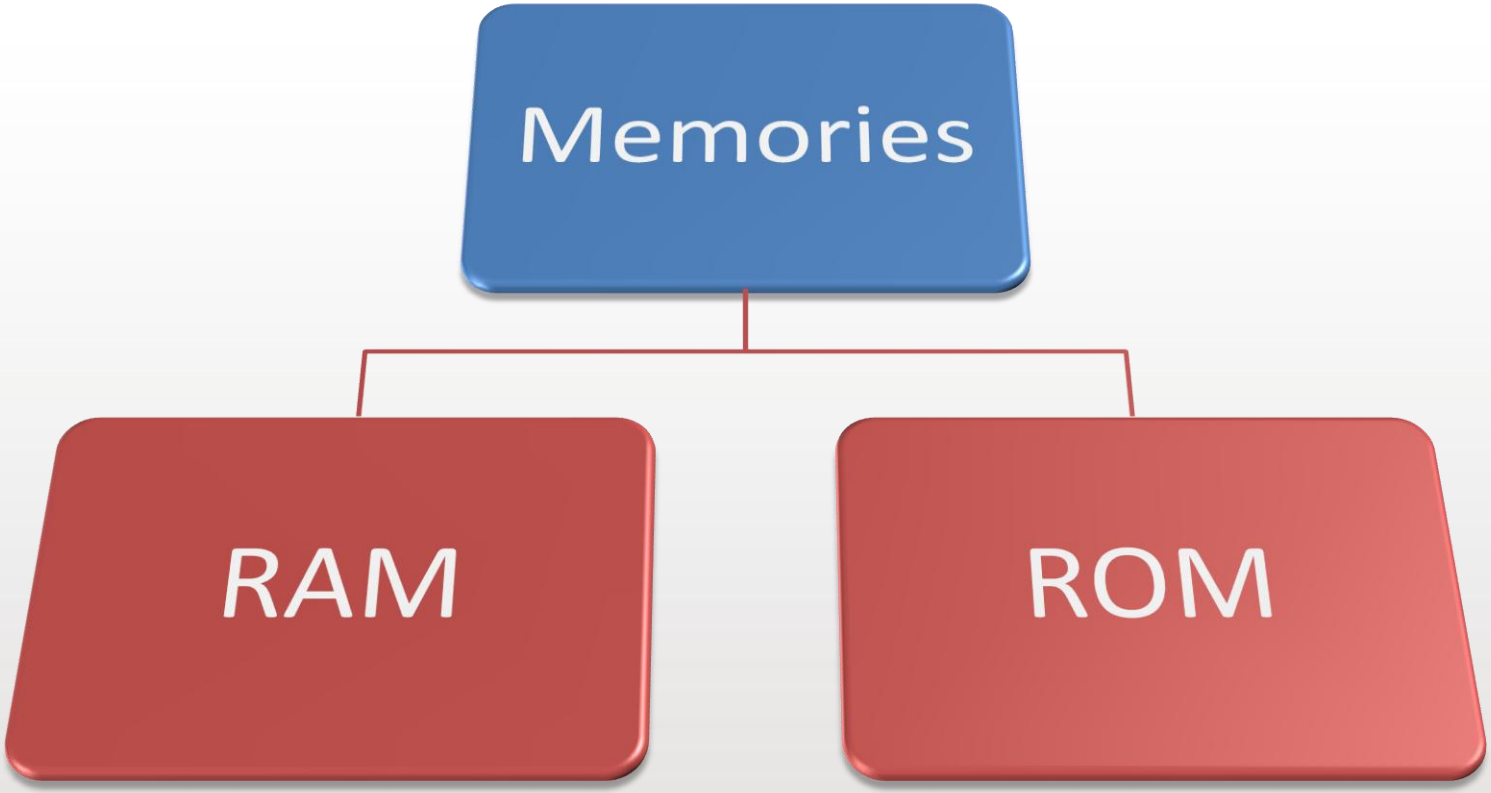
Digital Electronics (SKEE1223)

Memories and Programmable Logic Devices

Muhammad Arif Abd Rahim
Muhammad Mun'ím Ahmad Zabidi
Ab Hadi Abd Rahman

Faculty of Electrical Engineering


Logic Devices
Fixed
Memories
Programmable Logic Devices

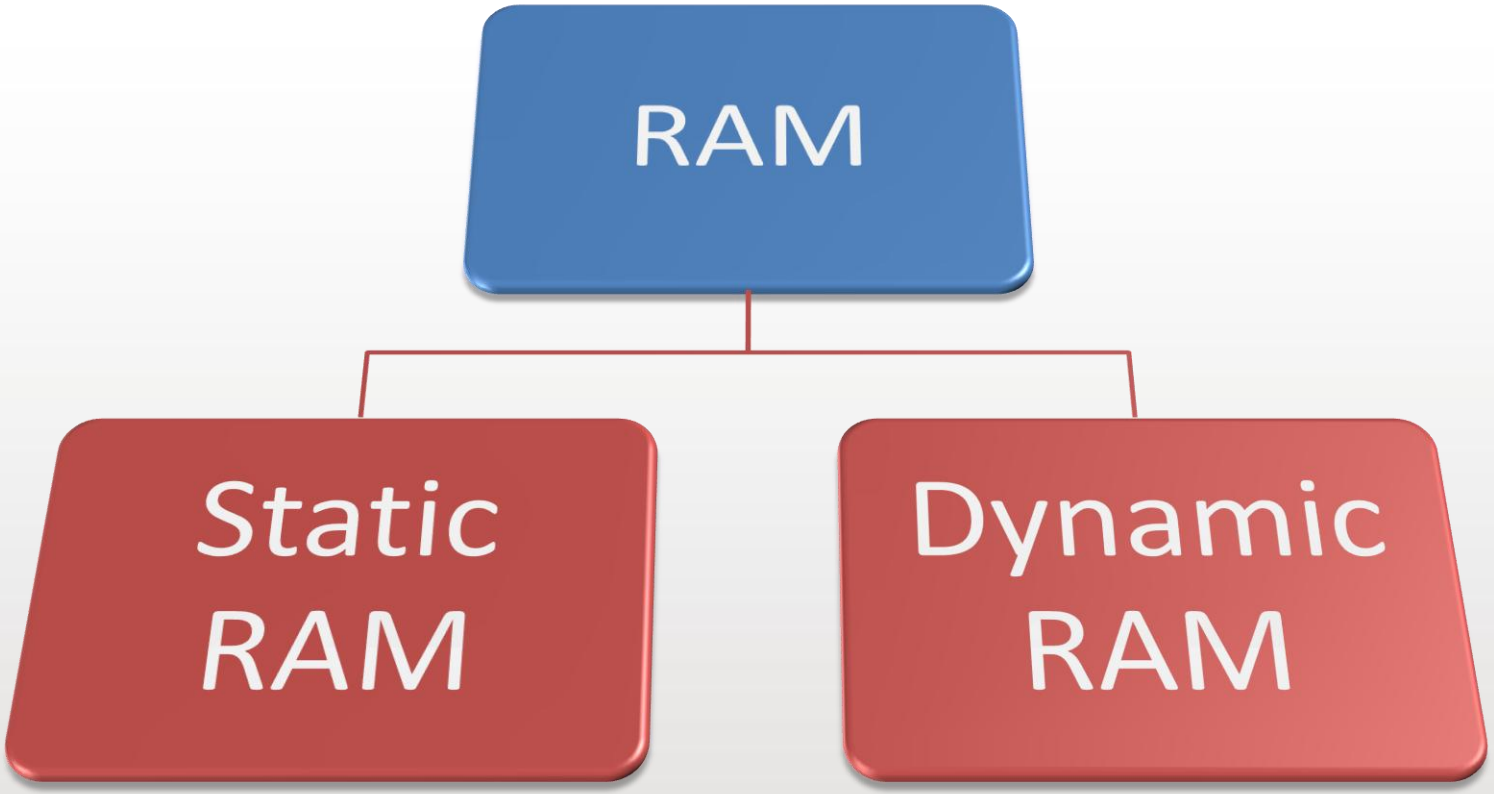

Memories
RAM
ROM

What are Memories?

- Memories store much more data than registers
- ROM
  - Read Only Memory
- RAM
  - Random Access Memory

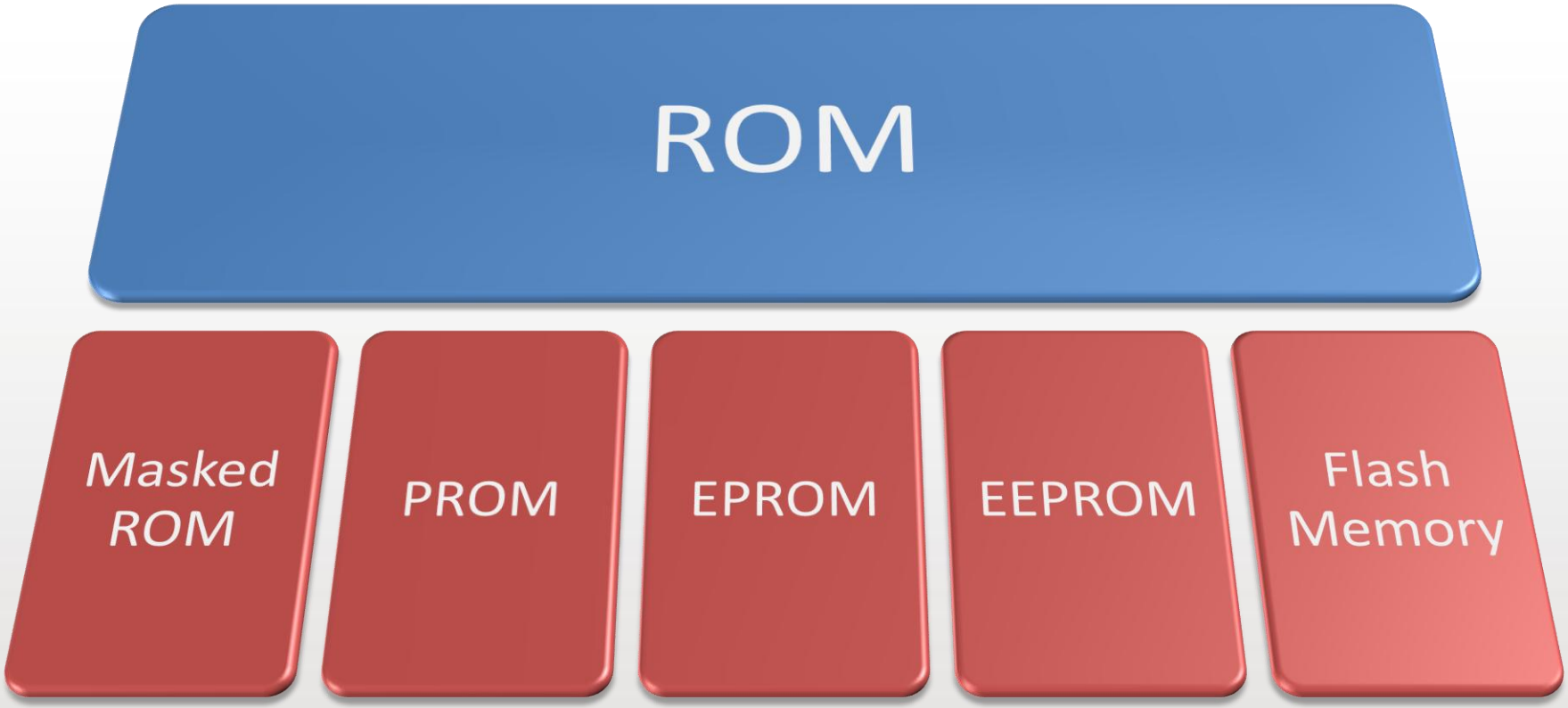
Memories

RAM	ROM
Random Access Memory	Read-Only Memory
Data erased when power is turned off	Data retained when power is turn off
Volatile	Non-volatile


RAM
Static RAM
Dynamic RAM

RAM

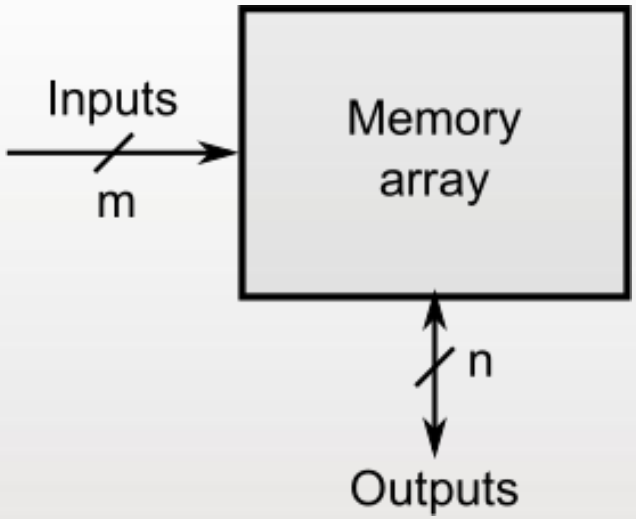
Static (SRAM)	Dynamic (DRAM)
Latch-based	Capacitor-based
Data retained as long as power is applied	Data is lost if not refreshed
Simpler to use	Requires external refresh circuit
More expensive	Cheaper
Lower capacity	Very high capacity


ROM
Masked ROM
PROM
EPROM
EEPROM
Flash Memory

ROM

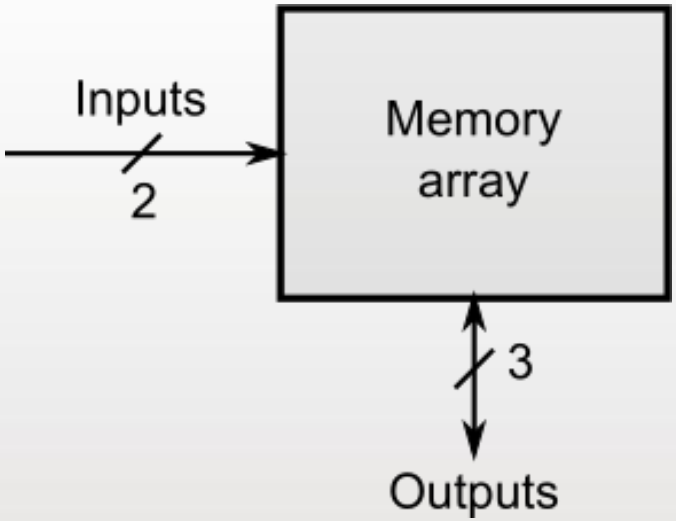
	Masked	PROM	EPROM	EEPROM	Flash
User Programming	Not possible	Once	Many times	Many times	Many times
Programming Cycle	Months	Minutes	Minutes	Seconds	Seconds
Density	High	Low	Low	Low	High

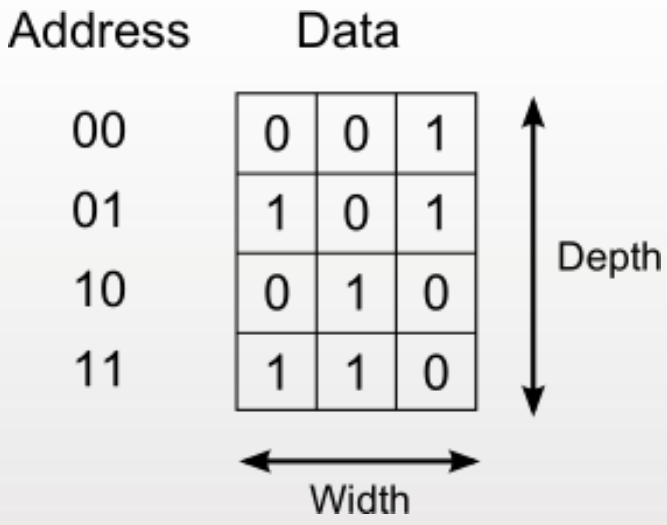
Generic *m* x *n* Memory



- *m* input lines
  → 2^m memory locations
- *n* output lines
- Total capacity
  – $2^m \times n$ bits

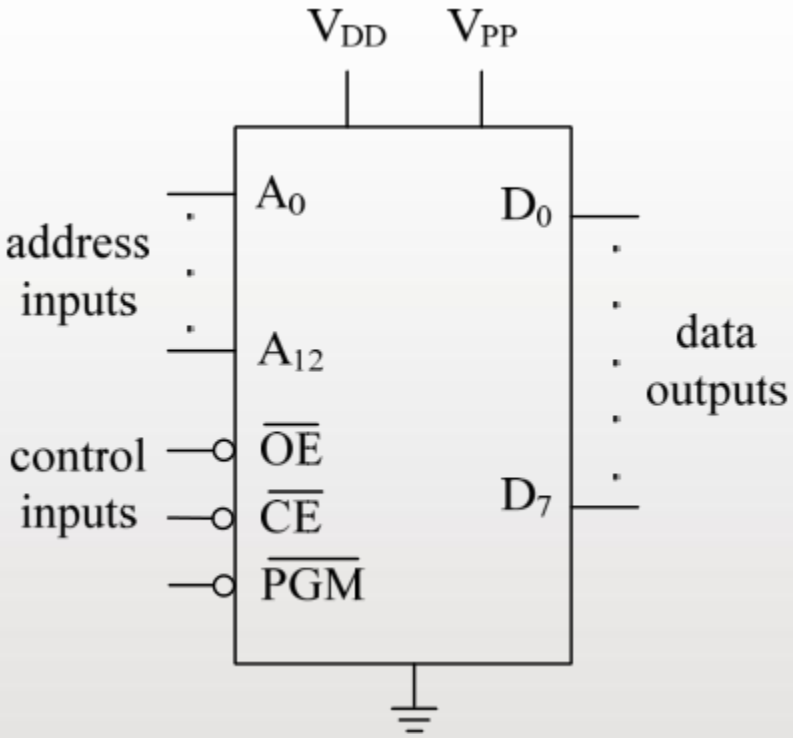
4 x 3 Memory


Inputs
2
Memory array
3
Outputs


Address
Data
00
01
10
11
0 0 1
1 0 1
0 1 0
1 1 0
Depth
Width

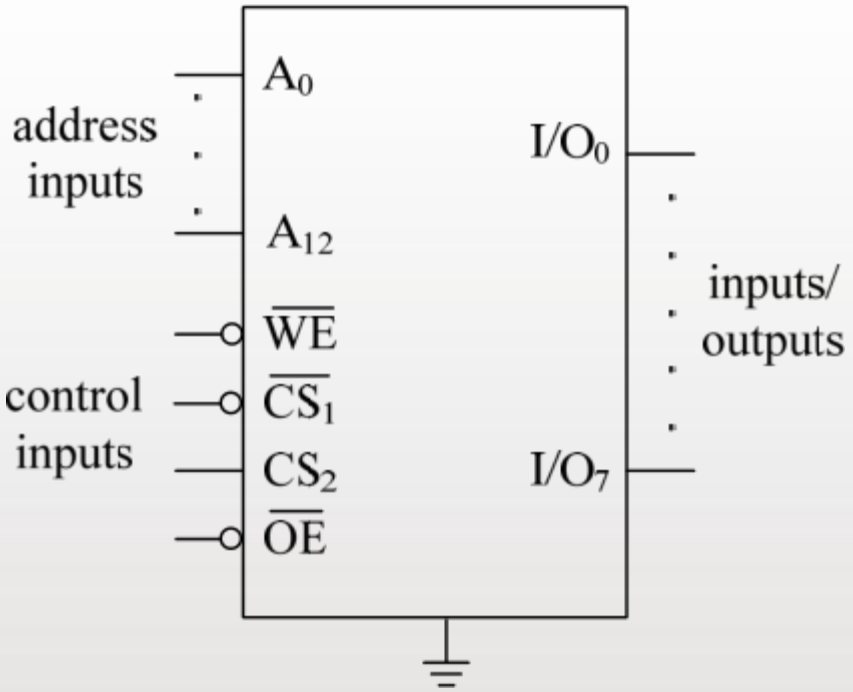
27C64 Device

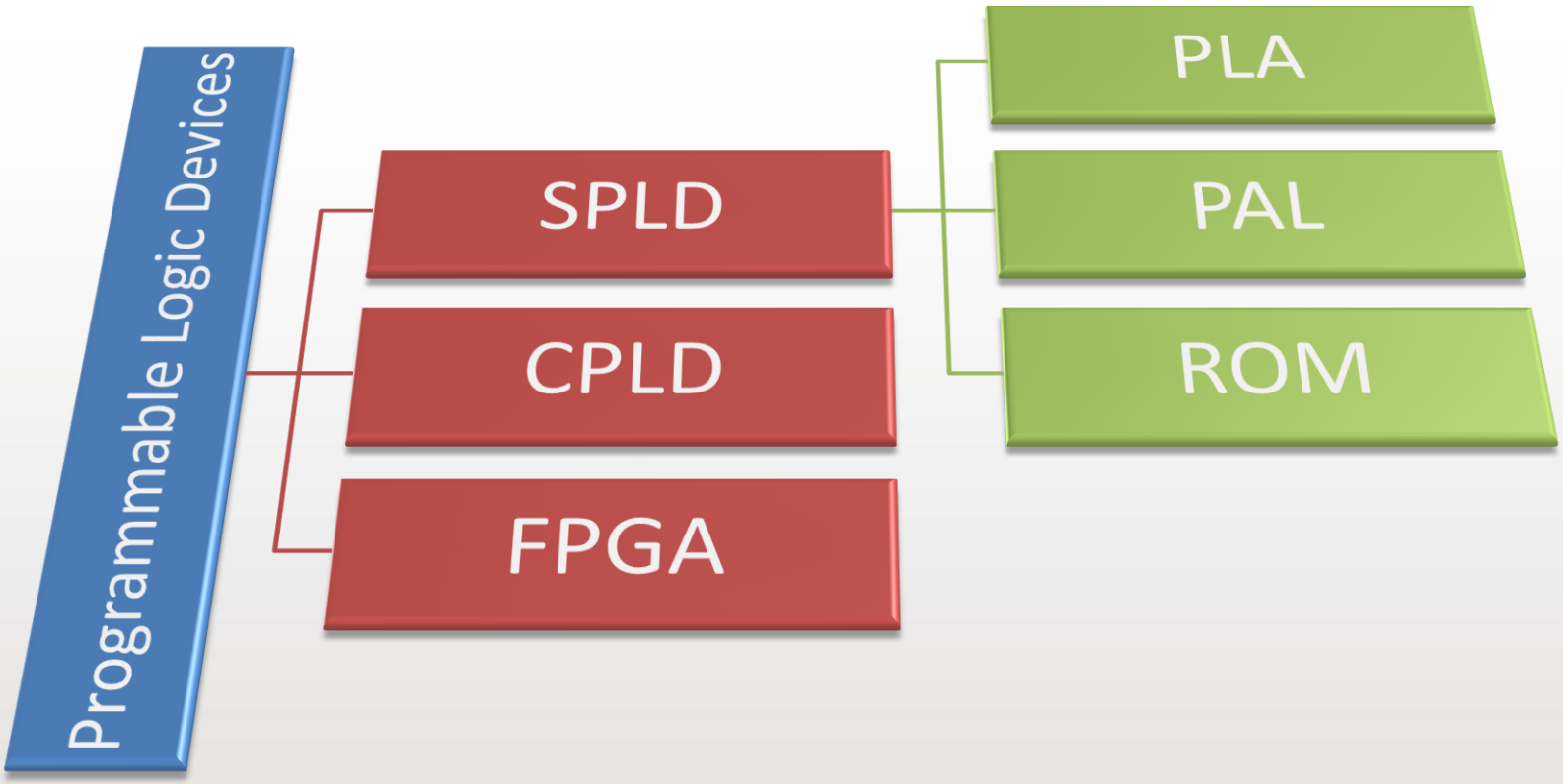
- 8192 x 8 EPROM
- 13 address lines
  → 2^{13} = 8192 = 8 kilo memory locations
- 64 kilobits capacity
- 8 data lines
- 2864 EEPROM has almost the same pinouts.



6264 Device

- 8192 x 8 SRAM
- 13 address lines
  → 2^{13} = 8192 = 8 kilo memory locations
- 8 data lines
- 64 kilobits capacity




Programmable Logic Devices
SPLD
CPLD
FPGA
PLA
PAL
ROM

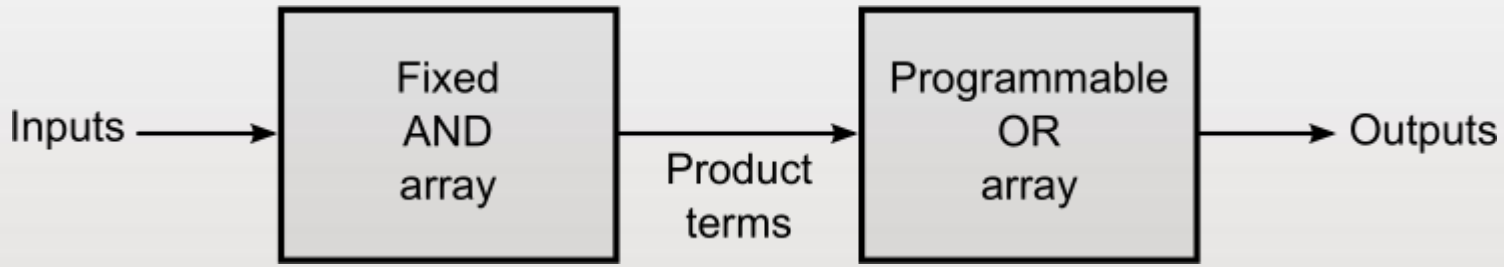
Programmable Logic Devices (PLD)

- **Sometimes called *Field Programmable Devices***

Acronym	Device	Complexity
SPLD	Simple Programmable Logic Device	Low
CPLD	Complex Programmable Logic Device	Medium
FPGA	Field Programmable Gate Array	High

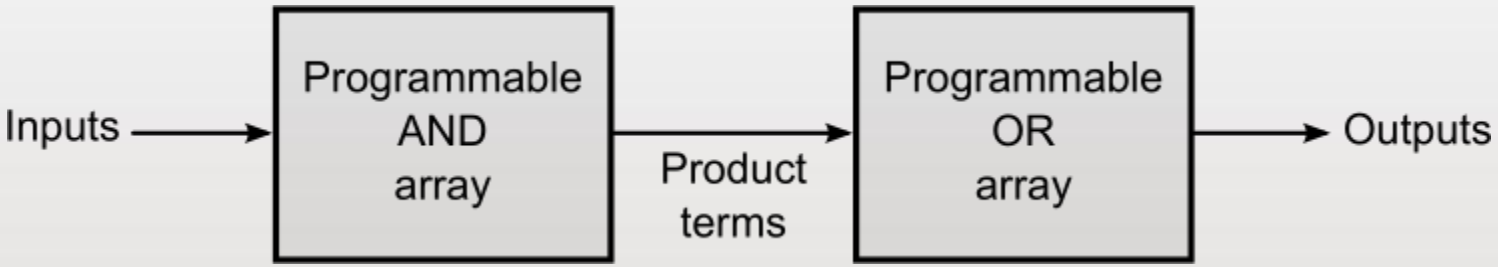
ROM

- *Read Only Memory*
- Good choice for implementing
  - Lookup tables
- Slow



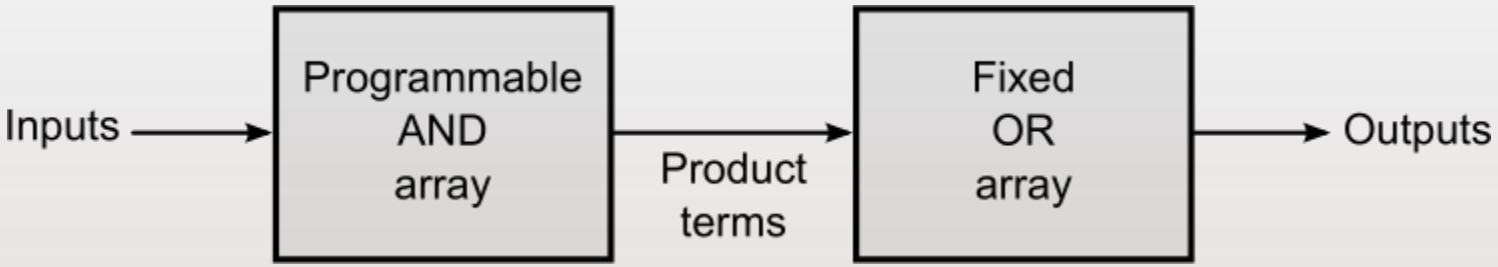
PLA

- *Programmable Logic Array*
- Good choice when many minterms are shared among the output function
- Expensive and relatively slow



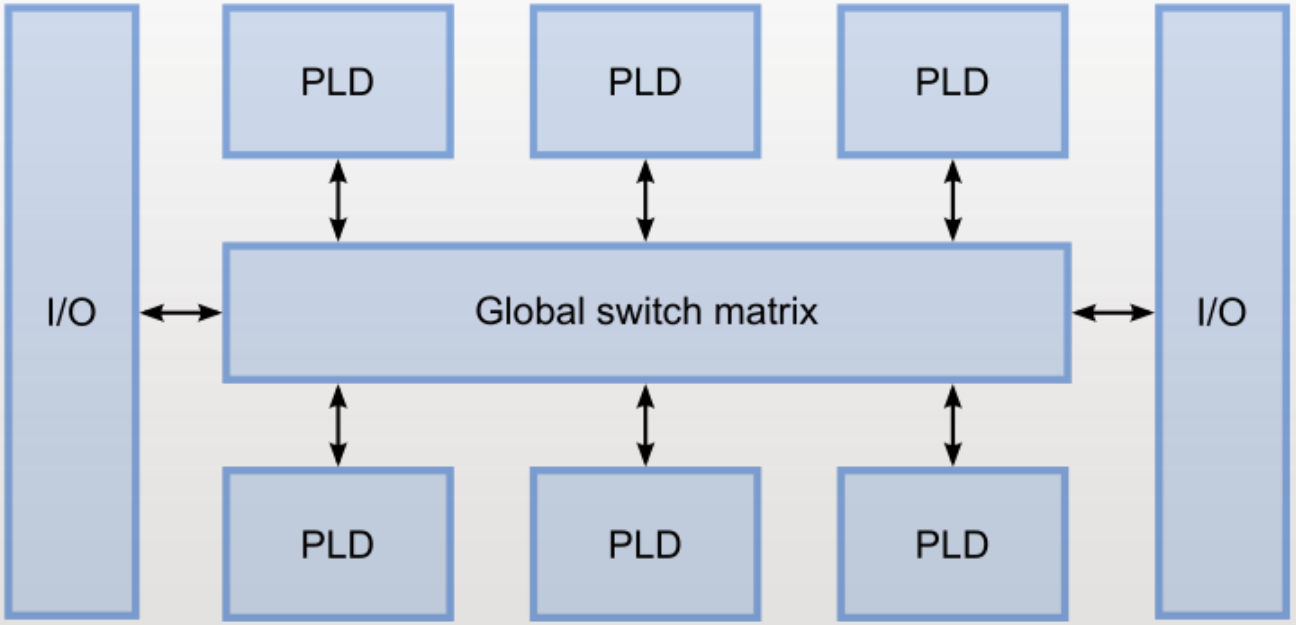
PAL

- *Programmable Array Logic*
- **Fastest type of SPLD**
- **Product terms cannot be shared, unlike PLA**



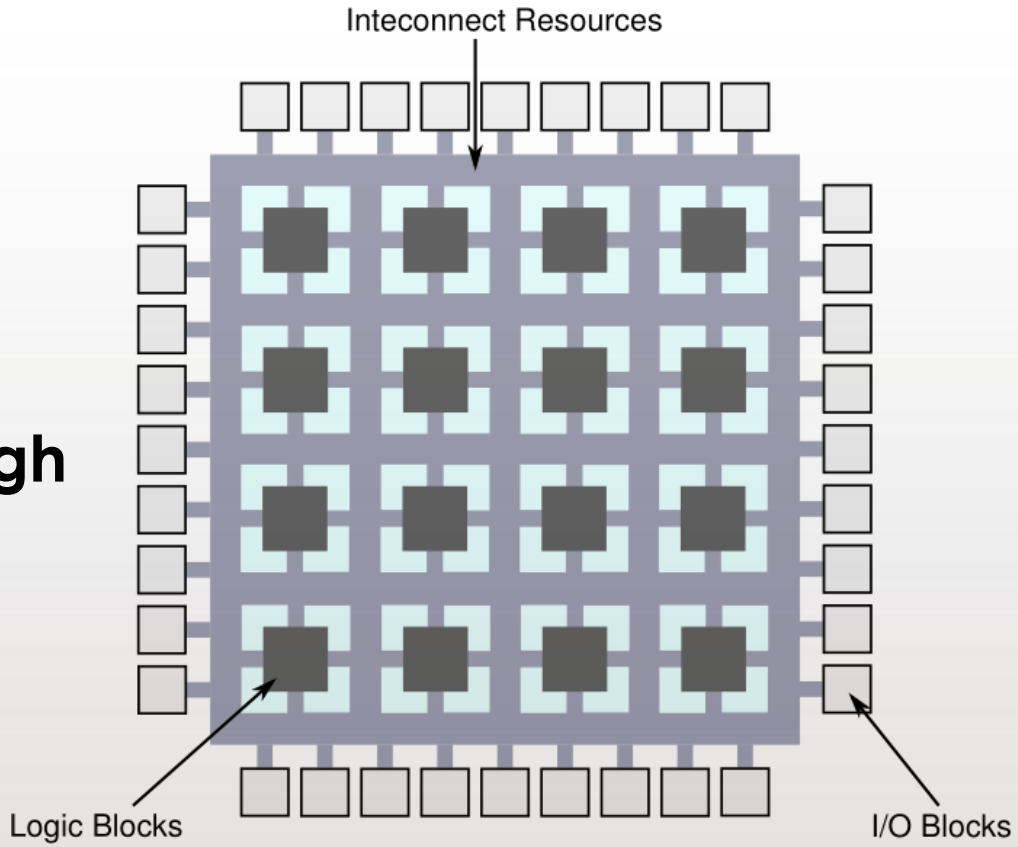
CPLD

- *Complex Programmable Logic Device*
- **PAL like blocks connected by an central interconnection network**



FPGA

- *Field Programmable Gate Array*
- Compared to CPLD:
  - Relative simple logic blocks
  - Connected through a distributed network
  - Up to millions of logic blocks



Tirjup Harimau / Tiger Shrike / Lanius tigrinus di Bidadari, Singapura