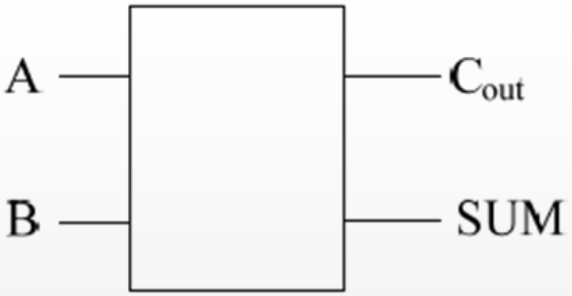
Digital Electronics (SKEE1223)

Standard Combinational Circuits II

Muhammad Arif Abd Rahim
Muhammad Mun'ím Ahmad Zabidi
Ab Hadi Abd Rahman

Faculty of Electrical Engineering

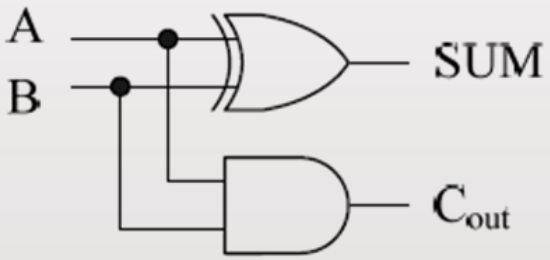
Half-Adder



(a) Logic symbol

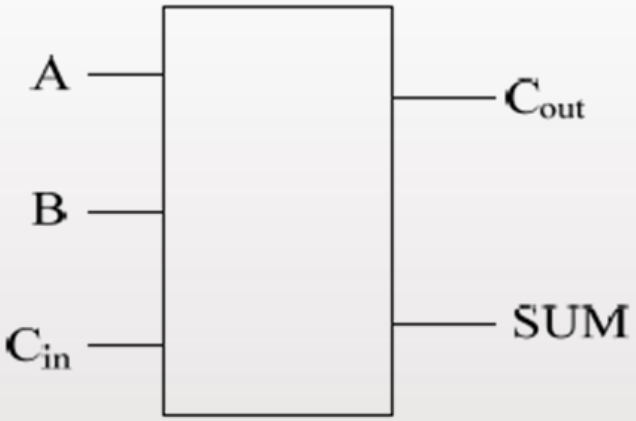
A	B	C_{out}	SUM
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

(b) Truth-table



(c) The circuit

Full-Adder

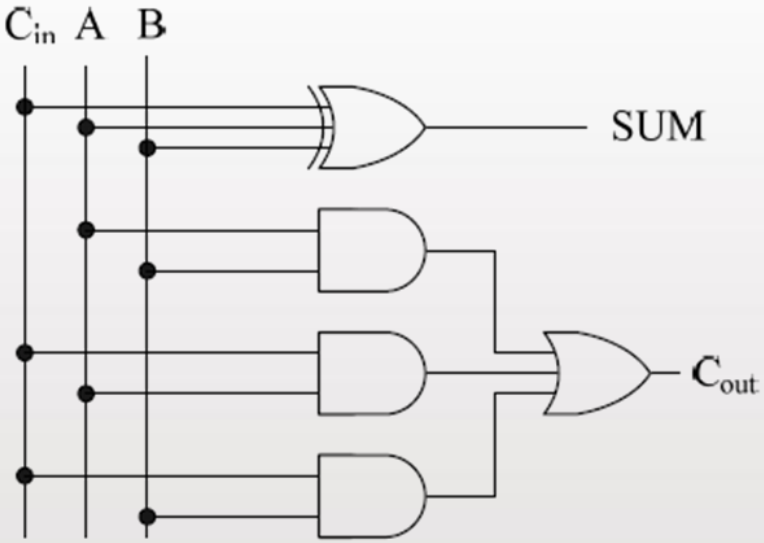


(a) Logic symbol

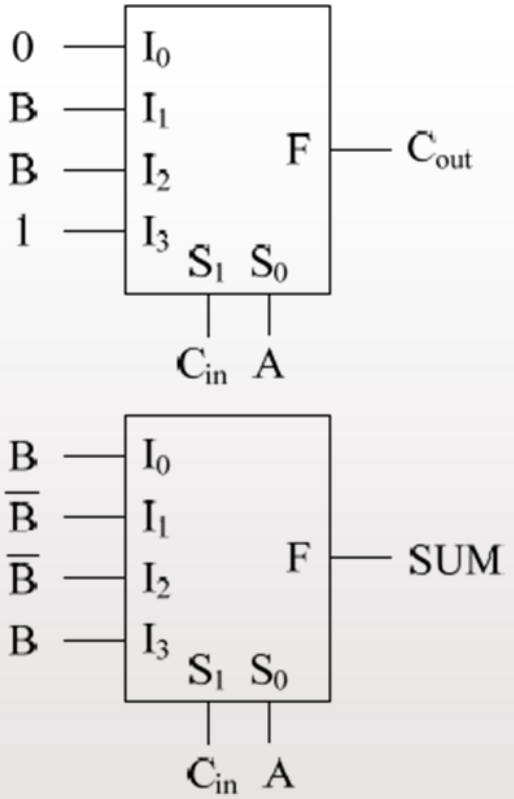
C_{in}	A	B	C_{out}	SUM
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

(b) Truth-table

Different Adder Implementations

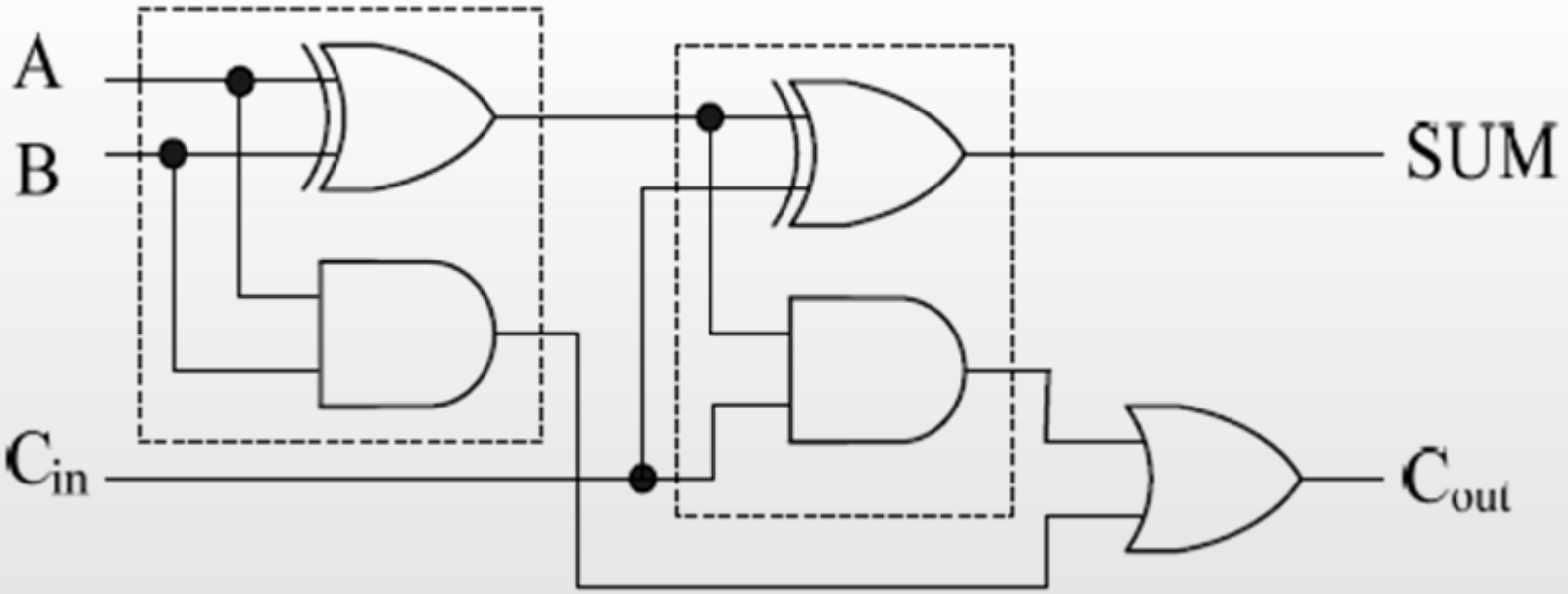


(a) logic gates

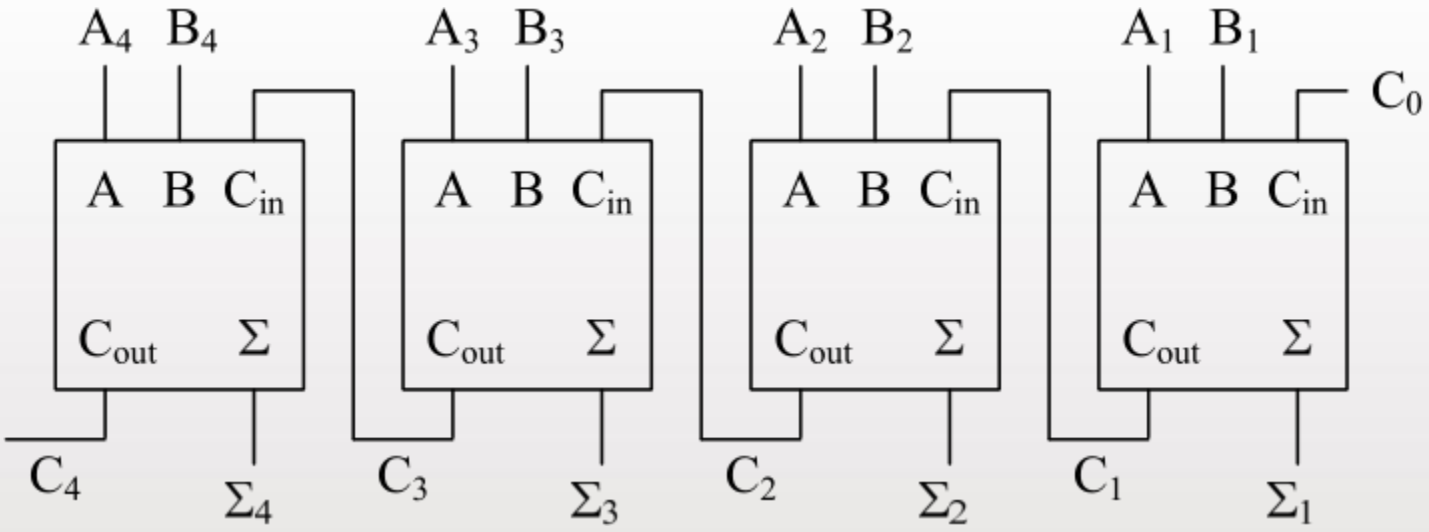


(b) 4 to 1 MUX

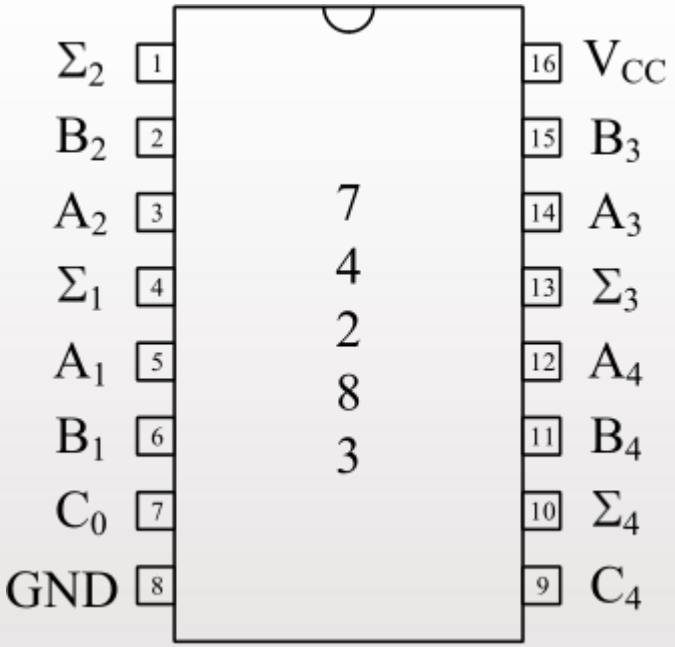
Adder Built Using "Half-Adders"

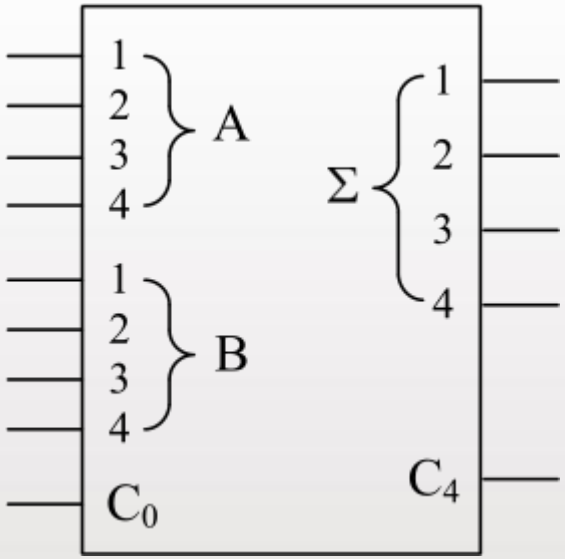


4-bit Parallel Adder



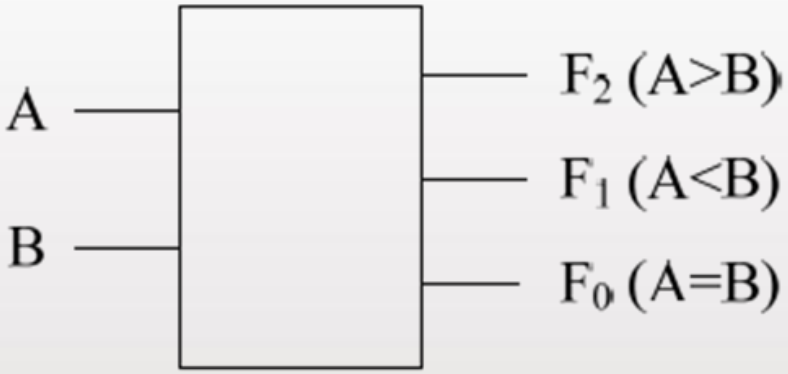
74283 Parallel Adder Chip





1-bit Comparator

1-bit comparator



logic symbol

A	B	F_2	F_1	F_0
0	0	0	0	1
0	1	0	1	0
1	0	1	0	0
1	1	0	0	1

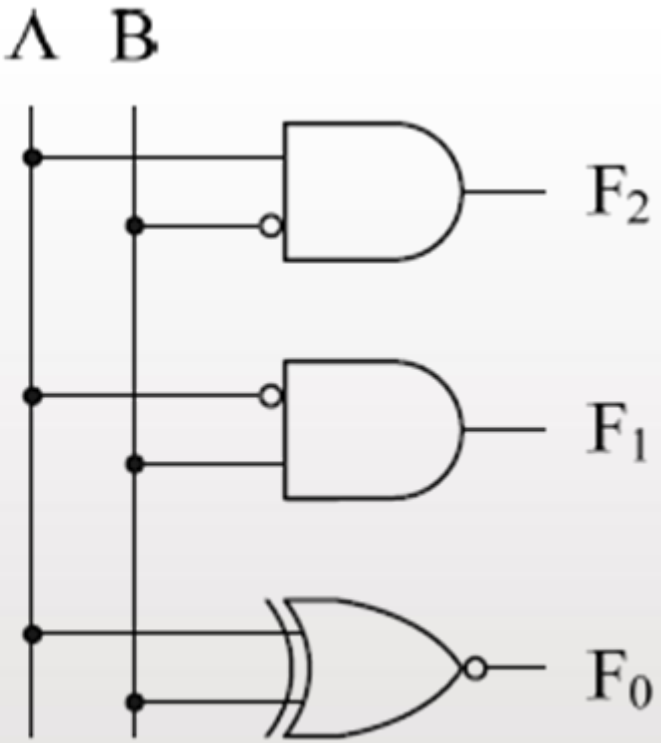
truth-table

1-bit Comparator

$$F_2 = A.\overline{B}$$

$$F_1 = \overline{A}.B$$

$$F_0 = \overline{A \oplus B}$$



4-bit Comparator Truth Table

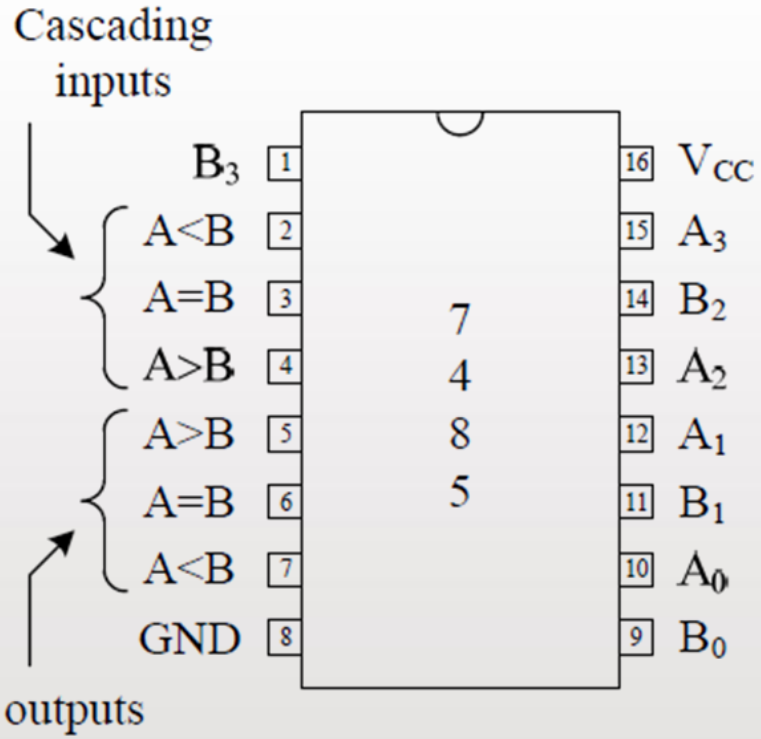
- 7485 chip (4-bit comparator)

Function Table

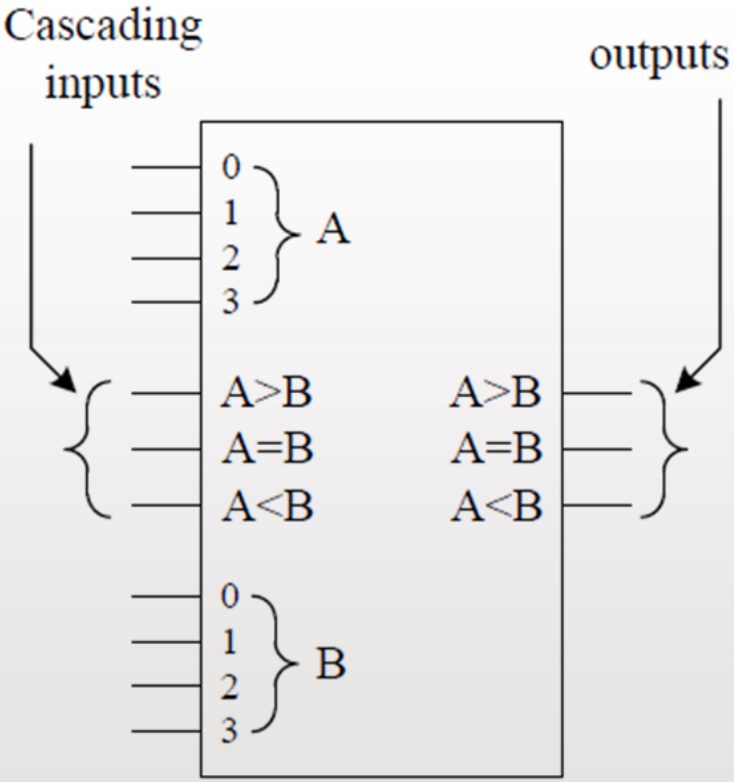
Comparing inputs				Cascading inputs			Outputs		
A_3,B_3	A_2,B_2	A_1,B_1	A_0,B_0	A>B	A<B	A=B	A>B	A<B	A=B
$A_3>B_3$	X	X	X	X	X	X	H	L	L
$A_3<B_3$	X	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2>B_2$	X	X	X	X	X	H	L	L
$A_3=B_3$	$A_2<B_2$	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	X	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0>B_0$	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	L	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	X	X	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	L	L	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L	H	H	L

H - High Level, L - Low Level, X - Don't care

Comparator Chip



Pin diagram



logic symbol